DIGITAL NOISE GENERATOR

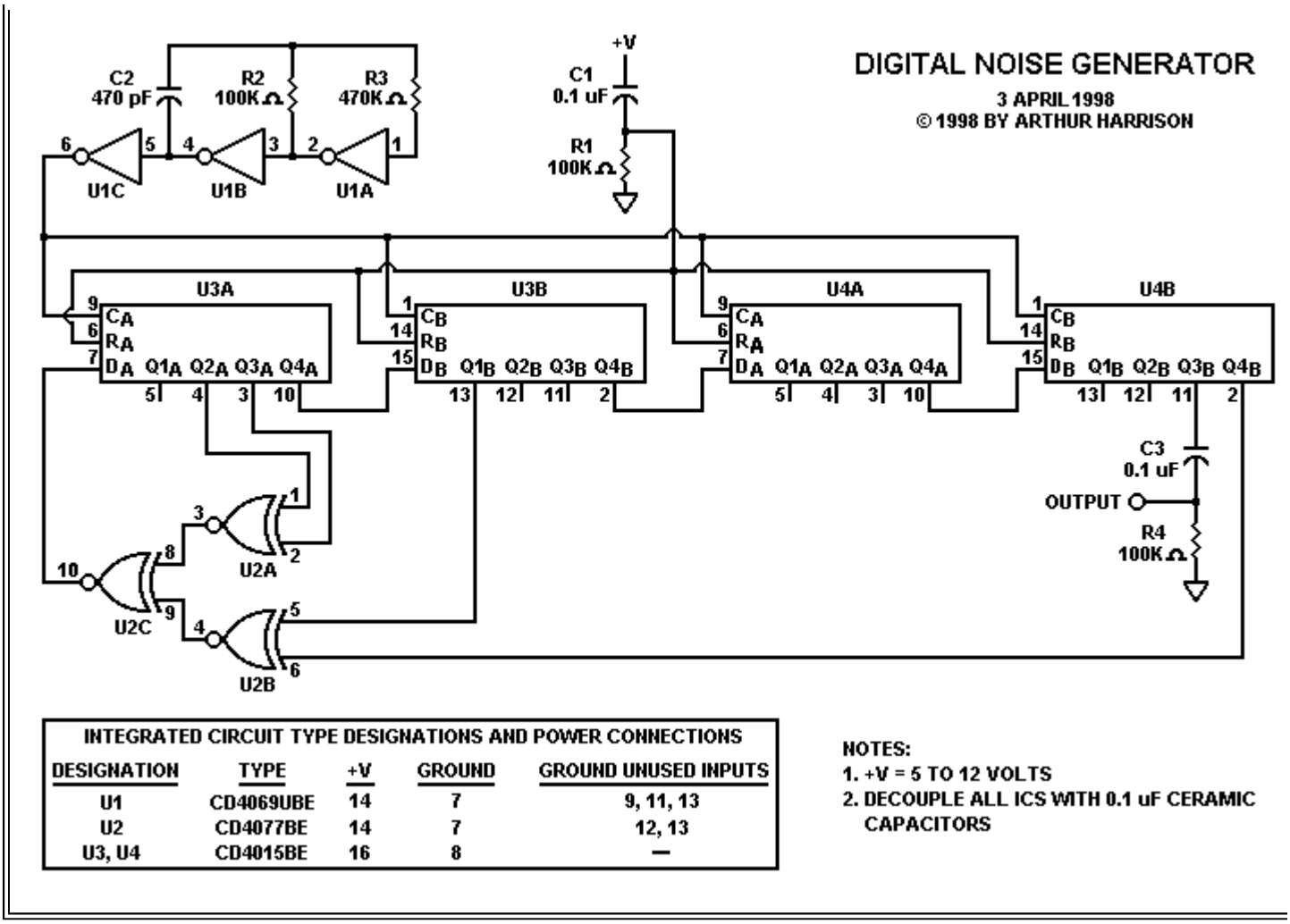
This circuit produces a repeating sequence of serial data that contains attributes useful for emulating audible noise. Upon power application, the momentary application of a "high" logic level is applied, via C1 and R1, to the RESET inputs of four four-bit shift registers, U3A, U3B, U4A, and U4B. These shift-register sections are serial-connected to form a single 16-bit register. The reset application causes the initial output states of the registers to be "low."

Four of the register outputs are connected to a group of exclusive-nor gates, U2A, B, and C, which produce a term at U2C's output, applied to the DATA input of the register at U3A pin 7. During the reset interval, this term is a logical "high," loaded into U3A on the first positive clock transition occurring after reset. Subsequent clock transitions cause this "high" state to transfer sequentially from one register output to the next. As the "high" state propagates through the register, it alters the data at the exclusive-nor network's output, and thus the register's DATA input. As the process continues, data resembling a random sequence is produced at each shift-register output. In fact, the sequence is not random, but rather the representation of the maximal-exponent polynomial expression, $1 + x^2 + x^3 + x^5 + x^{16}$. The shift-register output connections to the exclusive-nor gate array correspond directly to the exponent values in this expression.

Clocking is provided by U1, configured as a oscillator in conjunction with C2, R2, and R3. The values of C2 and R2 were selected to provide a clock frequency of about 8 kHz. Resistor R3 compensates for undesirable effects caused by the input-protection circuitry that is part of U1. The spectral spacing characteristic of the output waveform corresponds to $f_{clock} / (2^n)-1$, where n is equal to the number of stages in the shift register. For this configuration, the spectral spacing value is 0.1221 Hz. For many acoustic applications, the clock stability provided by the U1 circuit is sufficient, however, more predictable results may be obtained with a crystal-controlled clock. Timbre variations in the noise quality can be altered by varying the clock frequency.

The same data is presented at each shift-register output, delayed with relation to one another by a respective number of clock cycles. Output Q3B (pin 11 of U4B) was selected because it is otherwise unloaded by a exclusive-nor input, and conveniently accessed in a typical layout. The average output voltage at U4B, pin 11 is essentially one-half of the supply voltage. The output is AC-coupled via C3 and ground-referred via R4 for compatibility with following circuits, which may include analog filters and amplifiers.

This type of noise generator provides an advantage over noise-diode type circuits which depend on the extraction of noise from semiconductor junctions under specific conditions. Unit-to-unit parametric variations among such devices make repeatable designs costly and difficult, whereas the digital approach is easily repeatable, free from calibration, and inexpensive. The digital approach, however, being reiterative in nature, cannot substitute a noise diode circuit for providing purely random data.



INTEGRATED CIRCUIT TYPE DESIGNATIONS AND POWER CONNECTIONS				
DESIGNATION	TYPE	+V	GROUND	GROUND UNUSED INPUTS
U1	CD4069UBE	14	7	9, 11, 13
U2	CD4077BE	14	7	12, 13
U3, U4	CD4015BE	16	8	—

NOTES:
1. +V = 5 TO 12 VOLTS
2. DECOUPLE ALL ICS WITH 0.1 uF CERAMIC CAPACITORS

April 3, 1998

Back to the Circuit Library Index

Back to the Opening Page of Art's Theremin Page